* + H-Bridge Components:
    - MOSFET:
      * Why choose NMOS?
        + NMOS has lower Rds-on than PMOS; therefore lower power dissipation
        + NMOS are faster than PMOS; because electrons travel faster than holes
        + PMOS are more immune to noise; but that is not an issue for this application
      * Which NMOS to choose?
        + Must handle enough current (conservative estimate Id>20A)
        + Must tolerate enough voltage (conservative estimate Vds>30V)
        + Heat dissipation & Switching Frequency:
        + Low Rds-on means lower power dissipation in form of heat
        + BUT, the lower rdson gets, the bigger the MOSFET becomes. The bigger the physical device is, the bigger it’s gate will be. The gate forms a capacitor towards the source and the drain. Since MOSFETs are voltage driven devices, their gate-source voltage has to be in a certain range (usually above 5-10V) to be fully turned on, and in another range (less than a volt or so) to be turned off. So, the on and off transient has to charge and discharge these parasitic capacitors. If you have only limited current available to drive the gate (and you always do), the higher the gate-capacitance is, the longer it takes to charge or discharge it
        + ALSO, MOSFETs have a low rdson when they are fully on, and they conduct almost no current when they’re are completely off. In both cases the dissipated power is relatively low. However when they transition between these two states, there will be a short period where rdson is relatively high, but not high enough to stop significant current from flowing through the device. In these transitional periods both the voltage drop on the device (due to rdson) and the current through it are significant, resulting in high power-dissipation. Naturally you would like to keep this transition time as low as possible from this perspective (we’ll talk later about reasons why you don’t want it to be too fast either), so a higher gate-capacitance will not be desirable. With a given gate-drive strength the gate capacitance limits the speed by which the element can be turned on and off, and thus poses an operating frequency limit

<http://modularcircuits.tantosonline.com/blog/articles/h-bridge-secrets/mosfets-and-catch-diodes/>

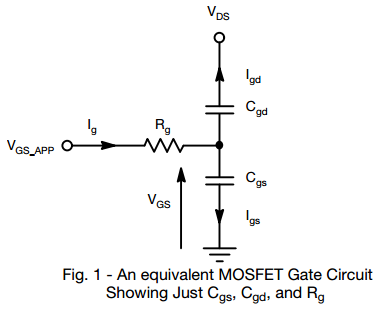
* + - * + For an N-channel device however the picture is more complicated. If you connect the gate to ground or to source, the device is opened (gate-source voltage is below or equal to 0). But where to connect it to close the device? The power supply is not enough, since, when the device is closed (conducts current), it’s source and drain are roughly at the same potential. Since the drain is connected to power, the source will be at that potential as well, but than gate should be **higher** than that to keep the device closed. In fact at minimum 5V higher for so-called logic-level MOSFETs and 10-15V higher for normal MOSFETs. This is a significant problem, that voltage somehow has to be generated. In most cases some kind of a charge-pump is used for that, either in a stand-alone or a boot-strapped configuration. The latter however is only useful if the bridge is driven in the ‘locked anti-phase’ mode (see later). In any case, these high-side drivers usually cannot deliver as much current as a regular low-side driver can, which means longer turn-on and -off times for the high-side (lower current takes longer to charge-discharge the gate-capacitance). In high-frequency operation, where switching loss is a significant factor, a P-channel MOSFET might be a better solution because of this. In low-frequency, high-current operation, where switching loss is not a problem, but channel-resistance is, N-channel transistors are usually a better compromise.

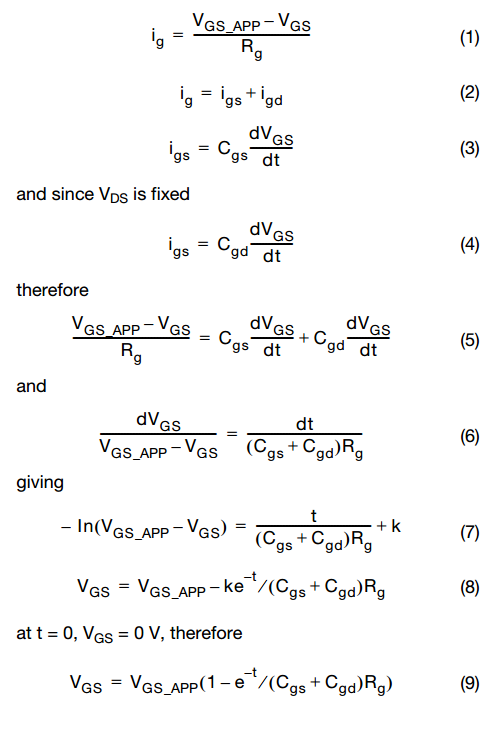
<http://modularcircuits.tantosonline.com/blog/articles/old-h-bridge-secrets/part-1/>

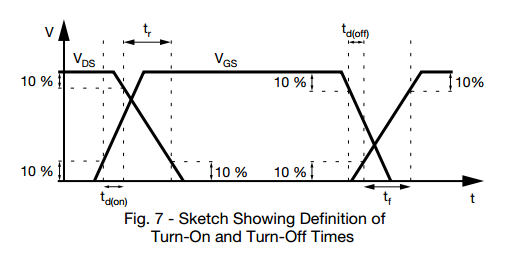
* + - * + The junction-to-ambient thermal resistance, that tells you how much hotter the chip is than the air that surrounds the package
        + The junction-to-case thermal resistance, that tells you how much hotter the chip inside the package is than the outside of the case at a certain power dissipation
        + the maximum allowed junction temperature
        + When working with surface-mount packages, it is important to note that thermal characteristics are highly dependent on the actual PCB layout. Take the traditional SO-8 package as an example (one typical FET datasheet is here for the [FDS8447](http://www.fairchildsemi.com/ds/FD/FDS8447.pdf)) You’ll see that with just the minimum amount of copper on the board the package has ~125oC/W thermal resistance. With a 6.5cm2 (1in2) copper area, the same number is less then half of this, ~50oC/W. Let’s say now that the device itself can operate up to 150oC (this is called the maximum allowed junction temperature). If you can keep the surrounding temperature (called ambient temperature) below 50oC, you can can dissipate somewhere between 0.8W ((150-50)/125) and 2W ((150-50)/50) of power on the FET depending on your PCB layout.

Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance

Application note 608 – Vishay Siliconix







the switching times of the MOSFET are affected not only by the parasitic elements, but also by the driving circuit.